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09/643,895	08/18/2000	Quinn A. Jacobson	SUN-P4914	8680

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EXAMINER	
O'BRIEN, BARRY J	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,895	JACOBSON ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5 and 7-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5 and 7-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-3, 5 and 7-18 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: RCE as received on 8/09/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Objections

5. Claim 18 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 18 defines a "native mode" as the capability to address each register of the backing register file via addresses or at random, while its parent claim, claim

12, also defines a "native mode" as the capability to address each register of the backing register file via addresses or at random. This is clearly not further limiting, as it is the same limitation.

6. Claim 14 is objected to because of the following informalities:

a. Claim 14 recites the limitation, "corresponding the backing register file instruction to a program" on its second line. This is not grammatically correct English, as the word "corresponding" cannot be used as a verb. Please correct the claim language to read more clearly.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 16 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 16 recites the limitation, "a new processor" on its second line. It is unclear whether "new" refers to a new technology, or to "new" as in out-of-the-box, i.e. a processor that has not been used before. Further, the specification has not explicitly defined "a new process" to be either of the above definitions (see p.18 of the Specification). Please correct the claim language to more clearly define the metes and bounds of the claim.

10. Claim 18 recites the limitation, "wherein a second mode is a native mode" on its first line. However, the parent claim of claim 18, claim 12, does not recite a "first mode", making it

unclear what this "second mode" is the second of. Please correct the claim language to more clearly define the metes and bounds of the claim.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-2, 5, 7-8 and 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by Sollars, U.S. Patent No. 5,900,025.

13. Regarding claim 1, Sollars has taught a processor comprising:

a. At least one register file (20a,b of Fig.1),

b. At least one execution unit (14 of Fig.1) coupled to the at least one register file (see Fig.1),

c. At least one bypass circuit operatively coupled to said at least one register file and said at least one execution unit, said at least one bypass circuit capable of arbitrating access to said at least one register file (see Col.3 lines 35-58 and Col.5 lines 32-54). Here, because arbitration of access to the register files amongst threads is occurring, there is inherently some circuitry associated with the arbitration process in order for it to be carried out.

d. A backing register file (22a of Fig.1) operatively coupled to said at least one register file (see Fig.1), and where said backing register file is operationally and

responsively coupled to at least one user-visible instruction (see Col.3 lines 25-34, Col.5 lines 21-31 and Col.14 lines 59-63), the user-visible instruction having registering windowing capability or having the capability to use the backing register file in a native mode, wherein the native mode is the capability to address each register of the backing register file by way of addresses or at random (see Col.14 lines 59-67). Here, it is inherent that the "MOV" instruction performs the same function as a backing register file instruction (see Col.14 lines 59-67), and that the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place using their register addresses (see Figs.16b and 16c). Because the claim uses the alternative format, only one of the alternative limitations is required to be met, and thus Sollars reads upon claim 1.

14. Regarding claim 2, Sollars has taught the processor as in claim 1, further comprising:

a. A plurality of register files (20a,b of Fig.1),

b. At least one execution unit operably connected to each register file of said plurality of register files (see Fig.1), and where said backing register file is operably connected to each register file of said plurality of register files (see Fig.1) providing thereby the ability to transfer values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files (see Col.3 lines 25-34).

15. Regarding claim 5, Sollars has taught a method for moving values from designated locations in designated register files (22a,b of Fig. 1) to designated locations in a backing register file (20a of Fig. 1) and values in designated locations in said backing register file to designated locations in designated register files (see Col.3 lines 25-34) comprising:

a. Identifying a backing register file instruction in a sequence of instructions, the sequence of instructions constituting one or more instruction streams, wherein the sequence of instructions has registering windowing capability or has the capability to use the backing register file in a native mode, wherein the native mode is the capability to address each register of the backing register file by way of addresses or at random (see Col. 14 lines 59-67). While not stated explicitly, it is inherent in the decoding operation (see Col.6 lines 16-18) that the instruction be identified, for without the identification of an instruction a computer would only be able to execute at most one type of instruction, effectively making it useless. Furthermore, it is inherent that the "MOV" instruction performs the same function as a backing register file instruction (see Col. 14 lines 59-67), and that the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place using their register addresses (see Figs. 16b and 16c). Because the claim uses the alternative format, only one of the alternative limitations is required to be met, and thus Sollars reads upon claim 5.

b. Decoding said backing register file instruction (see Col.6 lines 16-18), where if said backing file instruction is one of load-backing-register-file or load-register-

file, making available addresses for specified numbers of locations in specified register files and an equal number of addresses for specified locations in said backing register file, where said number of addresses is at least one. Because the instructions describe the transfer of data from one register to another (see Col.3 lines 25-34), it is inherent that not only must the instructions have at least one address for both the source and destination of the operation necessary for the instruction to execute encoded within the instruction, but that there is a minimal amount of decoding that is necessary in order to extract these addresses.

c. Reading values from each of said addresses ins said specified register file and writing said values to said equal number of addresses in said backing register file as specified by said backing register file instruction, if said backing register file instruction is of type load-backing-register-file. As described above, these instructions describe the transfer of data from one register to another (see above paragraph 18b and Col.3 lines 25-34). Therefore, it is inherent that in the execute stage of an instruction's lifecycle during a move/load-type instruction that the data is moved from one specified address to another specified address using the addresses specified in the decoded instruction.

d. Reading values form each of said addresses specified in said backing register file and writing said values to said equal number of addresses in said specified register file, if said backing register file instruction is of type load-register-file. As described above, it is inherent that move/load-type instructions transfer data from one specified address to a second specified address using addresses specified

in the decoded instruction (see above paragraphs 18b and 18c, and Col.3 lines 25-34).

16. Regarding claim 7, Sollars has taught a computer-readable medium containing an identifiable backing register file instruction for moving data between a memory and a backing register file, wherein the backing register file instruction has registering windowing capability or has the capability to use the backing register file in a native mode, wherein the native mode is the capability to address each register of the backing register file by way of addresses or at random (see Col.5 lines 25-34 and Col.14 lines 37-67). Here, it is inherent that the "MOV" instruction performs the same function as a backing register file instruction (see Col.14 lines 59-67), and that the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place using their register addresses (see Figs.16b and 16c). Because the claim uses the alternative format, only one of the alternative limitations is required to be met, and thus Sollars reads upon claim 7.

17. Regarding claim 8, Sollars has taught a computer-readable medium of claim 7, further comprising the backing register file instruction for transferring register values between a register file and said backing register file (see Col.3 lines 25-34 and Col.14 lines 37-67).

18. Regarding claim 10, Sollars has taught a computer-readable medium of claim 7, further comprising a structure for requesting instructions to be sent to the backing register file, wherein the structure is a linked list or a set of fields of specified length, the specified length being a plurality of bytes (see Col.6 lines 16-34). Here, the IFU fetches a plurality of instructions simultaneously, instructions which are a multiple bytes in size, and hence the instructions are a "set of fields" with a length of a "plurality of bytes". Furthermore, the instructions are "backing

register instructions" which move data between the register files and the backing register file (Col.3 lines 25-34). Therefore, since the claim language is in the alternate form, the limitations have been met by the prior art of record.

19. Regarding claim 11, Sollars has taught the processor of claim 1, further comprising the backing register file (22a of Fig.1) capable of being explicitly used by programs at all privilege levels (see Col.3 lines 25-58). Here, programs at a user level (see Col.3 lines 25-28), as well as well as all threads, can access all parts of the control register file (see Col.3 lines 45-58).

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 3, 9, and 12-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sollars, U.S. Patent No. 5,900,025 as applied to claims 1-2 above, and further in view of Wilhelm et al., U.S. Patent No. 5,956,747.

22. Regarding claim 3, Sollars has taught the processor as in claim 1, wherein the processor further comprises:

a. A connection circuit having a first connection, where said first connection is operably connected to said backing register file from the at least one register file (see Fig.1).

23. Sollars has not explicitly taught wherein the connection circuit further comprises a second connection, wherein said second connection is operably connected to a main memory from the said backing register file.

24. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Sollars and operably connect a main memory to the backing register file so that a non-trivial program can be stored and subsequently executed.

25. Regarding claim 9, Sollars has taught a computer-readable medium of claim 7, but has not explicitly taught wherein the computer-readable medium further comprises the backing register file instruction for transferring values between main memory and said backing register file.

26. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Furthermore, Official Notice is taken that it is well know in the art that instruction sets contain LOAD instructions in order to move program instructions from main memory into a register file. Therefore, one of ordinary

skill in the art would have found it obvious to modify the processor of Sollars and operably connect a main memory to the backing register file so that non-trivial program instructions can be stored in main memory, transferred to the backing register file using a LOAD instruction when needed and subsequently executed.

27. Regarding claim 12, Sollars has taught a method of accessing a backing register file (20a of Fig.1) comprising:

a. Identifying a backing register file instruction in an instruction stream, the identifying being the identification of an instruction for registering windowing capability or for using the backing register file in a native mode, wherein the native mode is the capability to address each register of the backing register file via addresses or at random (see Col.14 lines 59-67). While not stated explicitly, it is inherent in the decoding operation (see Sollars, Col.6 lines 16-18) that the instruction be identified, for without the identification of an instruction a computer would only be able to execute at most one type of instruction, effectively making it useless. Furthermore, it is inherent that the "MOV" instruction performs the same function as a backing register file instruction (see Col.14 lines 59-67), and that the instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place using their register addresses (see Figs.16b and 16c). Because the claim uses the alternative format, only one of the alternative limitations is required to be met, and thus Sollars reads upon claim 12.

b. Switching modes to access a backing register file (see Sollars Col.3 lines 35-58). Here, Sollars teaches switching the context (or mode) in order for threads to access the backing register file.

28. Sollars has not explicitly taught the method comprising the step of moving values between a main memory and a backing register file. However, Wilhelm has taught a register file (28 of Fig.2) and a register cache (52 of Fig.2) operably connected to a main memory (32 of Fig.2) so that the register values of the register file can be transferred to and stored in any backing memory (see Col.5 lines 1-11). One of ordinary skill in the art would have recognized that in order to execute a non-trivial program, some sort of instruction memory is necessary to hold the programs instructions. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Sollars and operably connect a main memory to the backing register file so that a non-trivial program can be stored in the main memory, transferred to the backing register file when needed and subsequently executed.

29. Regarding claim 13, Sollars in view of Wilhelm has taught the method of claim 12, wherein a first mode emulates a legacy software (see Sollars Col.1 lines 12-25). Here, the mode is switched between threads in order to access the backing register file (see Sollars Col.3 lines 35-58), and the backing register file can be used in a backward compatible emulation mode (see Sollars Col.1 lines 21-23).

30. Regarding claim 14, Sollars in view of Wilhelm has taught the method of claim 12, wherein identifying the backing register file instruction further includes corresponding the backing register file instruction to a program from which the backing register file instruction originates (see Sollars, Col.6 lines 16-34). Here, the fetching and decoding operations of the

processor inherently identifies which program a specific instruction came from, as such a feature is inherent in the operation of a multi-threaded processor so that data for each thread can be correctly identified and operated upon.

31. Regarding claim 15, Sollars in view of Wilhelm has taught the method of claim 12, wherein identifying the backing register file instruction further includes allowing full access to the backing register file after the identification of the backing register instruction (see Sollars, Col.14 lines 59-67). Here, the "MOV" instruction contains both source and destination fields allowing the user to identify the specific register from and to which the transfer will take place using their register addresses (see Sollars, Figs.16b and 16c).

32. Regarding claim 16, Sollars in view of Wilhelm has taught the method of claim 15, wherein allowing full access further includes using an extended instruction set or a standard instruction of a new processor (see Sollars, Col.14 lines 59-67). Here, because the processor of Sollars is a novel processor and contains the "MOV" instruction, it can be considered to be a standard instruction of a "new" processor (see above paragraph 9).

33. Regarding claim 17, Sollars in view of Wilhelm has taught the method of claim 15, wherein allowing full access further includes storing data in a structure, wherein the structure is a linked list or a byte stream (see Sollars, Col.14 lines 59-67). Here, the "MOV" instruction copies data between registers, which are "structure" in that they contain a "stream" of bytes.

34. Regarding claim 18, Sollars in view of Wilhelm has taught the method of claim 12, wherein a second mode is a native mode, wherein the native mode is the capability to address each register of the backing register file via addresses or at random (see Sollars, Col.14 lines 59-67). Here, the "MOV" instruction contains both source and destination fields allowing the user

to identify the specific register from and to which the transfer will take place using their register addresses (see Sollars, Figs. 16b and 16c).

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (571) 272-4171. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm, with the exception of first Friday of every bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached at (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
10/19/2004

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